In The Claims:

Claims 1-14 (previously withdrawn)

Claim 15. (Currently Amended) A thin film transistor structure, comprising:

an insulating substrate;

a polysilicon layer over the substrate;

a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer, a gate dielectric layer between the gate layer and the polysilicon layer and a spacer on each side of the gate layer, wherein the spacer with respect to a surface of the gate ~~dielectric~~ layer and a surface of the polysilicon layer forms a contrast surface; and

a selective conductive layer over the gate layer and the polysilicon layer adjacent to the spacers based on the contrast surface, wherein the selective conductive layer on the polysilicon layer adjacent to the spacers directly serves as a source/drain region ~~without additionally implanting process on the source/drain region~~.

Claim 16. (original) The structure of claim 15, wherein the polysilicon layer has a thickness between about 250Å to 350Å.

Claim 17. (original) The structure of claim 15, wherein the conductive layer comprises an in-situ doped silicon-germanium (SiGe) layer.

Claim 18. (original) The structure of claim 15, wherein the conductive layer comprises a tungsten layer.

Claim 19. (orginal) The structure of claim 15, wherein the conductive layer comprises a metal silicide layer.

Claim 20. (original) The structure of claim 15, wherein the spacer comprises a tetra-ethyl-ortho-silicate (TEOS) layer.